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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,080	01/30/2001	Nobutaka Taniguchi	100353-00037	8190

7590 03/21/2006

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EJL

Office Action Summary	Application No.	Applicant(s)	
	09/772,080	TANIGUCHI ET AL.	
	Examiner	Art Unit	
	Kevin M. Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the amendment filed 2/15/2006, is a final office action.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/15/2006 has been entered.

3. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Response to Arguments

4. Applicant's arguments filed 2/15/2006 have been fully considered but they are not persuasive. Applicant states Wang (or Wang and Hanke) fails to teach or suggest adjusting a delay time of the input signal so as to match the phases of a signal input to an input buffer that supplies the input signal to the delay adjusting circuit (PLL circuit) and a signal output from an output buffer that outputs an output signal from the PLL circuit. However, the combination of Wang (or Wang and Hanke) and the instant application's disclosed prior art discloses these limitations as stated in the previous office actions and stated below. Applicant further states, if the signal output from the output buffer were fed back to the PLL circuit via a dummy circuit, the performance of the PLL circuit would deteriorate when the output pattern is not a constant toggle between high and low levels. The examiner disagrees. The dummy circuit receives a clock signal from frequency divider 4 in figure 1 of the instant application's disclosed prior art. The dummy circuit outputs a delay clock signal dclk. This output will be a constant toggle between high and low levels.

5. Applicant has added limitations to the claims. These limitations are addressed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 6,448,820) in view of the instant application's disclosed prior art, specifically figure 1.

Regarding claims 8, 10 and 11, Wang discloses a delay adjusting circuit in a phase locking loop shown in figure 5. A variable delay circuit is disclosed in element 533. This delay circuit is implemented using a number of buffers or inverters connected in a ring oscillator arrangement (column 6, lines 61-63). The delay circuit 533 outputs a signal to the divider 539. The divider 539 generates clock feedback to the phase comparator 516. The divider circuit divides the frequency of the clock output by an amount from 1 to about 256 (column 7, lines 1-4). The phase comparator compares the phases of the input signal and the frequency divided feedback signal (figure 5 and column 7, lines 5-20). The output of the phase comparator 516 outputs signals to the charge pump. The charge pump will output a control signal 529 to adjust some delay cells 533 to maintain lock or phase relationship (column 6, lines 58-60). The frequency of the divided signal can be less than the frequency of the input signal. The PLL will attempt of lock these signals to the same frequency. In addition, the divider circuit has a divider ratio that is programmably selectable (column 12, lines 8-9). The frequency

divided feedback signal will ideally be equal to the REF CLOCK input signal so no adjustment need take place. The dividing of the feedback signal helps to minimize the phase adjustment necessary in the circuit.

Wang does not disclose using an input buffer, an output buffer and a dummy circuit to delay a signal from the frequency divider by a fixed delay time. However, the instant application's disclosed prior art shows, in figure 1, the input and output buffers and a dummy circuit delaying the signal from the frequency divider. It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the buffers and dummy circuit of the instant application's disclosed prior art into the delay adjusting circuit of Wang. The dummy circuit allows the signal propagation delay to be equal so the phase relationship of the feedback clock signal and the input clock signal will be the same. The fixed delay will allows that only small adjustments to be made in the delay cells of Wang reducing the complexity of that circuitry.

7. Claims 3, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 6,448,820) in view of Hanke, III et al (US 5,376,848) further in view of the instant application's disclosed prior art, specifically figure 1.

Regarding claims 3, 7 and 9, Wang discloses a delay adjusting circuit in a phase locking loop shown in figure 5. A variable delay circuit is disclosed in element 533. This delay circuit is implemented using a number of buffers or inverters connected in a ring oscillator arrangement (column 6, lines 61-63). The delay circuit 533 outputs a signal to the divider 539. The divider 539 generates clock feedback to the phase comparator 516.

The divider circuit divides the frequency of the clock output by an amount from 1 to about 256 (column 7, lines 1-4). The phase comparator compares the phases of the input signal and the frequency divided feedback signal (figure 5 and column 7, lines 5-20). The output of the phase comparator 516 outputs signals to the charge pump. The charge pump will output a control signal 529 to adjust some delay cells 533 to maintain lock or phase relationship (column 6, lines 58-60). The frequency of the divided signal can be less than the frequency of the input signal. The PLL will attempt of lock these signals to the same frequency. In addition, the divider circuit has a divider ratio that is programmably selectable (column 12, lines 8-9). The frequency divided feedback signal will ideally be equal to the REF CLOCK input signal so no adjustment need take place. The dividing of the feedback signal helps to minimize the phase adjustment necessary in the circuit. Wang does not disclose dividing the input signal by a first division rate. Hanke discloses a delay matching circuit shown in figures 5 and 6. Figure 6 discloses a divider circuit capable of dividing the input signal by a number of values to ensure the input signal and the output signal are phase matched. It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the teaching of Hanke into the apparatus and method of Wang. By dividing the input frequency, the original signal is locked to the output signal and a more accurate delay adjustment is formed (column 8, lines 31-37). When the feedback signal matches the divided REF CLOCK input to the phase/frequency detector, no adjustment is necessary.

The combination of Wang and Hanke does not disclose using an input buffer, an output buffer and a dummy circuit to delay a signal from the frequency divider by a fixed

delay time. However, the instant application's disclosed prior art shows, in figure 1, the input and output buffers and a dummy circuit delaying the signal from the frequency divider. It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the buffers and dummy circuit of the instant application's disclosed prior art into the delay adjusting circuit of the combination of Wang and Hanke. The dummy circuit allows the signal propagation delay to be equal so the phase relationship of the feedback clock signal and the input clock signal will be the same. The fixed delay will allows that only small adjustments to be made in the delay cells of the combination reducing the complexity of that circuitry.

Conclusion

8. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
3/18/2006

KEVIN BURD
PRIMARY EXAMINER